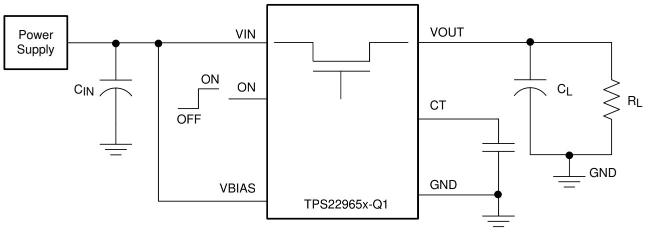
TPS22965x-Q1 5.5V、4A、16mΩ 导通电阻负载开关

1 特性

- 符合汽车类应用 要求
  - 符合 AEC-Q100 标准
  - 器件温度等级 2：-40°C 至 +105°C（TPS22965-Q1、TPS22965N-Q1）
  - 器件温度等级 1：-40°C 至 +125°C（TPS22965W-Q1、TPS22965NW-Q1）
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C6
- 提供功能安全
  - 可帮助进行功能安全系统设计的可用文档
- 集成单通道负载开关
- 输入电压范围：0.8V 至 5.5V
- 超低导通电阻 (R_{ON})
  - V_{IN} = 5V（V_{BIAS} = 5V）时，R_{ON} = 16mΩ
  - V_{IN} = 3.6V（V_{BIAS} = 5V）时，R_{ON} = 16mΩ
  - V_{IN} = 1.8V（V_{BIAS} = 5V）时，R_{ON} = 16mΩ
- 4A 最大持续开关电流
- 低静态电流 (50µA)
- 低控制输入阈值支持使用 1.2V、1.8V、2.5V 和 3.3V 逻辑器件
- 可配置的上升时间
- 快速输出放电 (QOD)（仅限 TPS22965-Q1 和 TPS22965W-Q1）
- 带有散热焊盘的 WSON 8 引脚封装

简化电路原理图



2 应用

- 汽车电子产品
- 信息娱乐
- ADAS（高级驾驶辅助系统）

3 说明

TPS22965x-Q1 是一款具有受控导通功能的小型、超低 R_{ON} 单通道负载开关。此器件包含一个可在 0.8V 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET，并且支持 4A 的最大持续电流。VOUT 上升时间是可配置的，因此可以减小浪涌电流。TPS22965-Q1 和 TPS22965W-Q1 器件包括一个 225Ω 片上负载电阻，用于在开关关闭时快速输出放电。

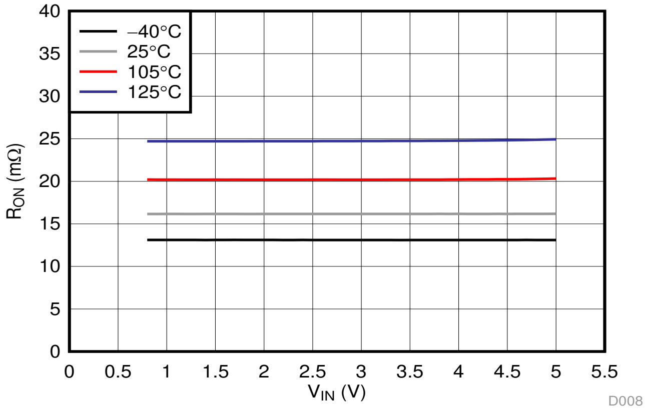
TPS22965x-Q1 器件采用节省空间的 2mm × 2mm 8 引脚 WSON 小型封装 (DSG0008A)，带有集成散热焊盘，可实现较高的功率耗散。TPS22965-Q1 和 TPS22965N-Q1 器件可在 –40°C 至 105°C 的自然通风温度范围内正常运行。此外，TPS22965W-Q1 和 TPS22965NW-Q1 器件采用相同的 WSON 封装（DSG0008B），具有可湿性侧面。其可在 –40°C 至 +125°C 的自然通风温度范围内正常工作。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TPS22965-Q1	DSG0008A WSON (8)	2.00mm × 2.00mm
TPS22965N-Q1		
TPS22965W-Q1	DSG0008B WSON (8)	
TPS22965NW-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

R_{ON} 与 V_{IN} 之间的关系（V_{BIAS} = 5V，I_{OUT} = –200mA）



English Data Sheet: SLVSCI3

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (September 2016) to Revision D	**Page**
• 将“提供功能安全”连接添加到了 *特性* 部分	1

Changes from Revision B (December 2015) to Revision C	**Page**
• 已添加 更改了*说明* 部分和 *Thermal Information* 表中的封装标识符。	1

Changes from Revision A (June 2015) to Revision B	**Page**
• 将 TPS22965W-Q1 器件的状态更新为“正在供货”。	1
• Added 125°C temperature performance to typical AC timing parameters	12

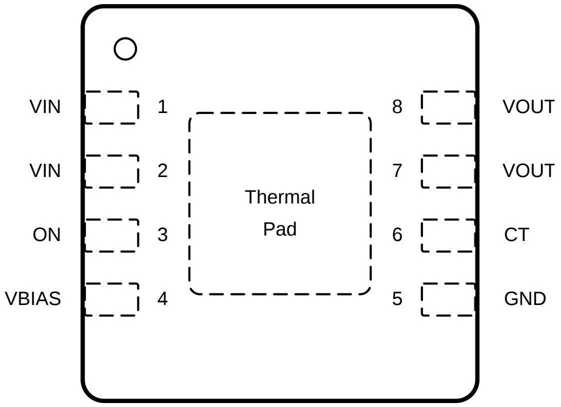
Changes from Original (April 2014) to Revision A	**Page**
• 已添加 TPS22965N-Q1 器件型号。	1
• Updated Thermal Information table.	5
• Updated typical AC timing parameters (tables, graphs and scope captures)	12

5 Device Comparison Table

DEVICE	R_{ON} AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE	PACKAGE WITH WETTABLE FLANKS	MAXIMUM OUTPUT CURRENT	TEMPERATURE RANGE
TPS22965-Q1	16 mΩ	Yes	No	4 A	–40°C to +105°C
TPS22965N-Q1	16 mΩ	No	No	4 A	–40°C to +105°C
TPS22965W-Q1	16 mΩ	Yes	Yes	4 A	–40°C to +125°C
TPS22965NW-Q1	16 mΩ	No	Yes	4 A	–40°C to +125°C

6 Pin Configuration and Functions

**DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1 2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Application and Implementation* section for more information
7 8	VOUT	O	Switch output
—	Thermal pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT (2)
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	On voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		6	A
T_J	Maximum junction temperature		150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.5	V
V_{ON}	ON voltage		0	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C_{IN}	Input capacitor		1 (1)		µF
T_A	Operating free-air temperature (2)	TPS22965N-Q1, TPS22965-Q1	–40	105	°C
		TPS22965NW-Q1, TPS22965W-Q1	–40	125	

(1) See the *Application and Implementation* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{J\theta A}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} × P_{D(max)})$

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS22965-Q1, TPS22965N-Q1	TPS22965W-Q1, TPS22965NW-Q1	UNIT
		DSG0008A (WSON)	DSG0008B (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	67.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	95	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 5 V		–40°C to +105°C		50	75	µA
				–40°C to +125°C		50	75	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to +125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +105°C		0.2	8	µA
				–40°C to +125°C			36	
			V_{IN} = 3.3 V	–40°C to +105°C		0.02	3	
				–40°C to +125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to +125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.005	1	
				–40°C to +125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	

Electrical Characteristics—V_{BIAS} = 5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			28	
			V_{IN} = 3.3 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.8 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.5 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 1.2 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
			V_{IN} = 0.8 V	25°C		16	23	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			25	
				–40°C to +105°C 965NW-Q1, 965W-Q1			26	
				–40°C to +125°C			27	
R_{PD} (1)	Output pull-down resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +105°C		225	300	Ω
				–40°C to +125°C		225	300	

(1) TPS22965-Q1 and TPS22965W-Q1 Only

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature:
–40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1).
Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_{Q} V_{BIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		–40°C to +105°C		20	30	µA
				–40°C to 125°C		20	30	
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
				–40°C to 125°C			2	
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +105°C		0.01	3	µA
				–40°C to 125°C			13	
			V_{IN} = 1.8 V	–40°C to +105°C		0.01	2	
				–40°C to 125°C			6	
			V_{IN} = 1.2 V	–40°C to +105°C		0.005	2	
				–40°C to 125°C			6	
			V_{IN} = 0.8 V	–40°C to +105°C		0.003	1	
				–40°C to 125°C			4	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
				–40°C to +125°C			0.5	

Electrical Characteristics—V_{BIAS} = 2.5 V (continued)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature: –40°C ≤ T_A ≤ +105°C (TPS22965N-Q1, TPS22965-Q1), –40°C ≤ T_A ≤ +125°C (TPS22965NW-Q1, TPS22965W-Q1). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		20	26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to 105°C 965NW-Q1, 965W-Q1			32	
				–40°C to +125°C			34	
			V_{IN} = 1.8 V	25°C		19	26	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			28	
				–40°C to +105°C 965NW-Q1, 965W-Q1			30	
				–40°C to +125°C			32	
			V_{IN} = 1.5 V	25°C		18	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1/965W-Q1			29	
				–40°C to +125°C			31	
			V_{IN} = 1.2 V	25°C		18	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
			V_{IN} = 0.8 V	25°C		17	25	mΩ
				–40°C to +105°C 965N-Q1, 965-Q1			27	
				–40°C to +105°C 965NW-Q1, 965W-Q1			28	
				–40°C to +125°C			30	
R_{PD} (1)	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +105°C		275	325	Ω
				–40°C to +125°C		275	330	

(1) TPS22965-Q1 and TPS22965W-Q1 only

7.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). These switching characteristics are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1600		µs
t_{OFF}	Turnoff time			9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1985		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		3		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		660		µs
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		730		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		100		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		380		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		560		µs
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2435		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		9		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		2515		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		4		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1230		µs
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1565		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		70		µs
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		930		µs
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		8		µs
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF, C_{IN} = 1 µF		1110		µs

7.8 Typical Characteristics

7.8.1 Typical DC Characteristics

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

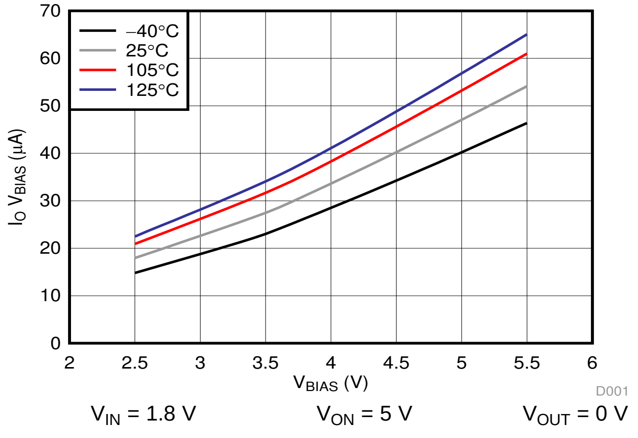


Figure 1. V_{BIAS} Quiescent Current vs V_{BIAS}

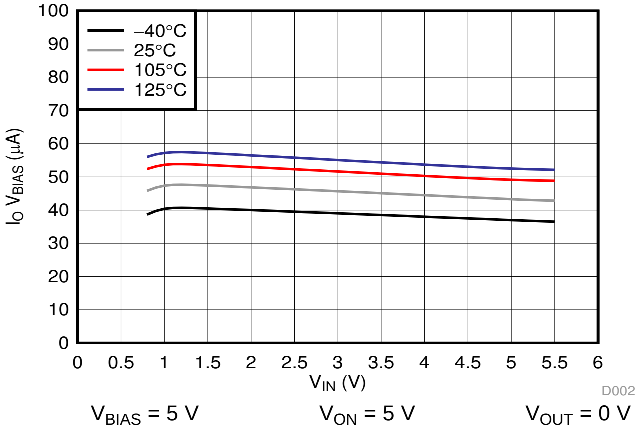


Figure 2. I_Q V_{BIAS} vs V_{IN}

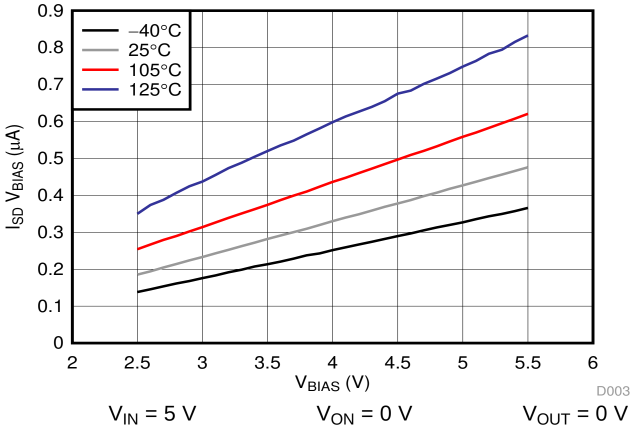


Figure 3. I_{SD} V_{BIAS} vs V_{BIAS}

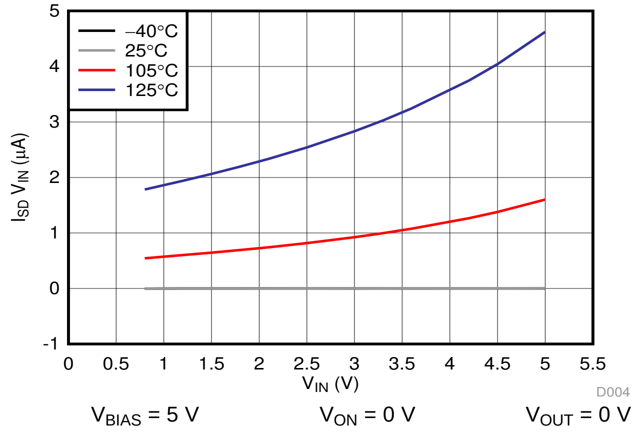


Figure 4. I_{SD} V_{IN} vs V_{IN}

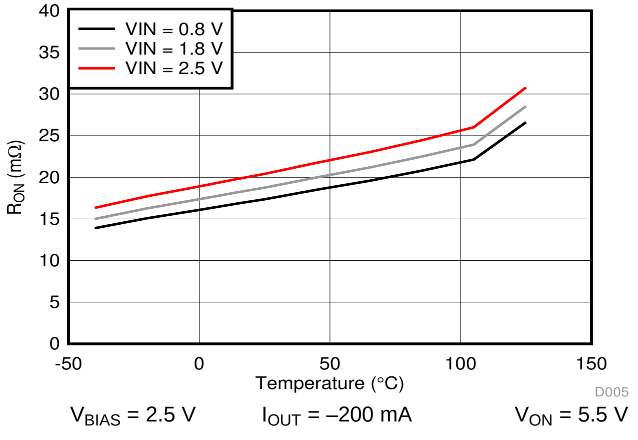
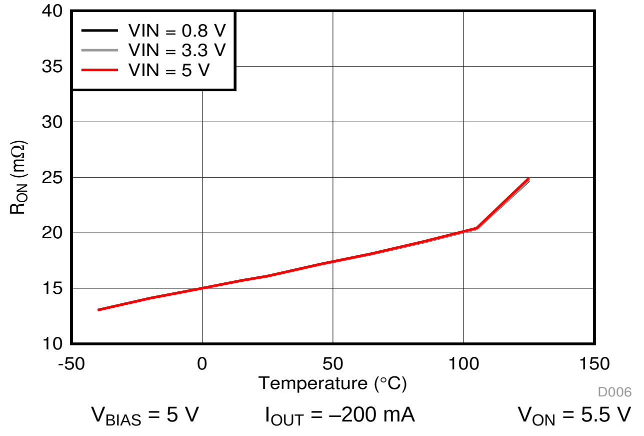


Figure 5. R_{ON} vs Ambient Temperature

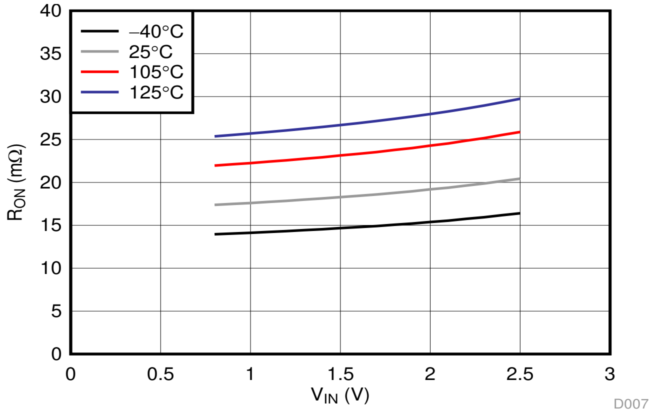


Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

Figure 6. R_{ON} vs Ambient Temperature

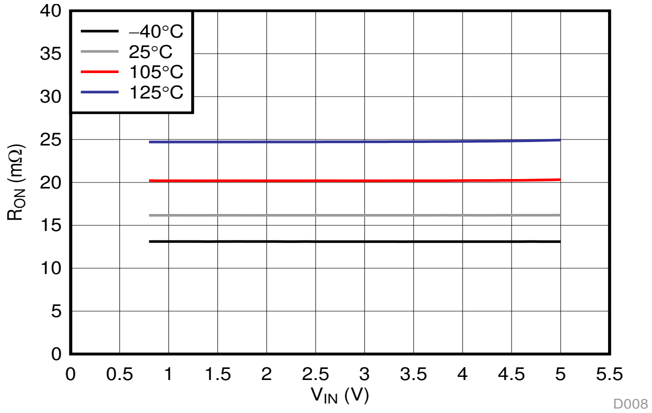
Typical DC Characteristics (continued)

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



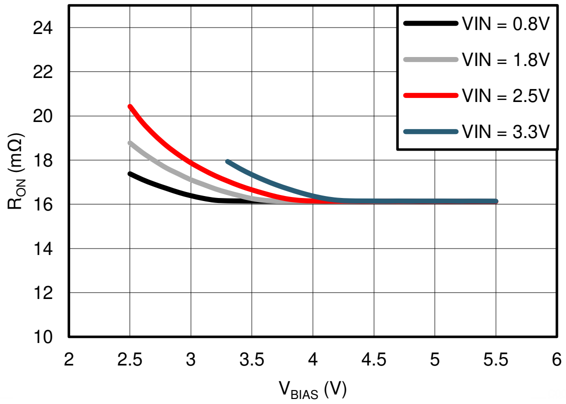
V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 7. R_{ON} vs V_{IN}



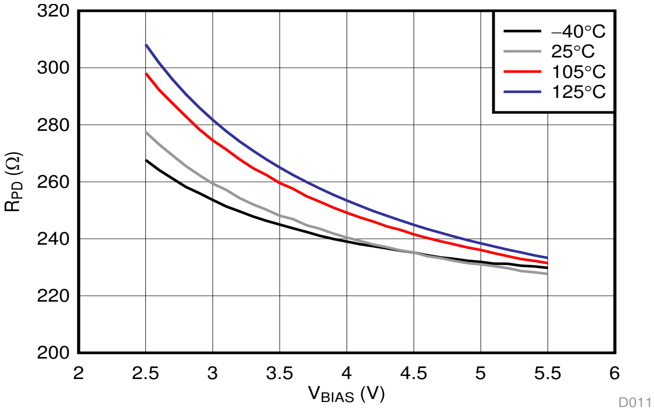
V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 8. R_{ON} vs V_{IN}



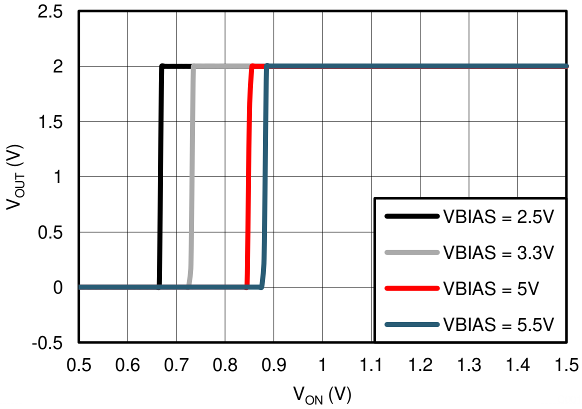
T_A = 25°C I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 9. R_{ON} vs V_{BIAS}



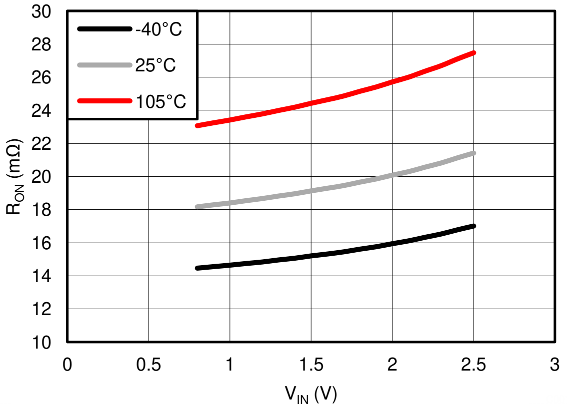
V_{IN} = 1.8 V V_{ON} = 0 V

Figure 10. R_{PD} vs V_{BIAS}



V_{IN} = 2 V T_A = 25°C

Figure 11. V_{OUT} vs V_{ON}



V_{BIAS} = 2.5 V I_{OUT} = –4 A V_{ON} = 5.5 V

Figure 12. R_{ON} vs V_{IN}

Typical DC Characteristics (continued)

T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

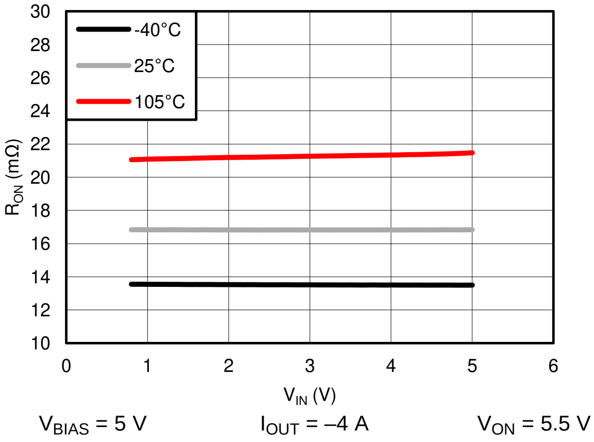


Figure 13. R_{ON} vs V_{IN}

7.8.2 Typical Switching Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.

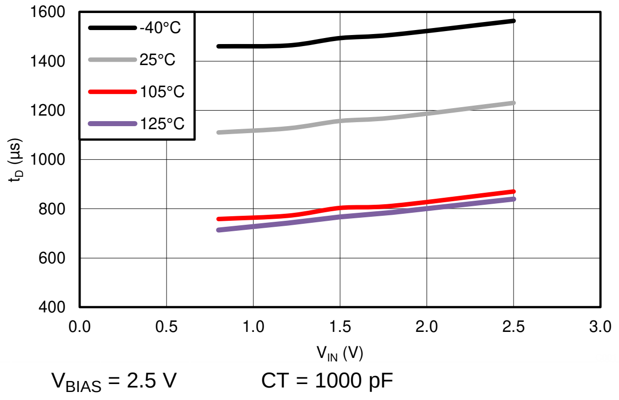


Figure 14. t_D vs V_{IN}

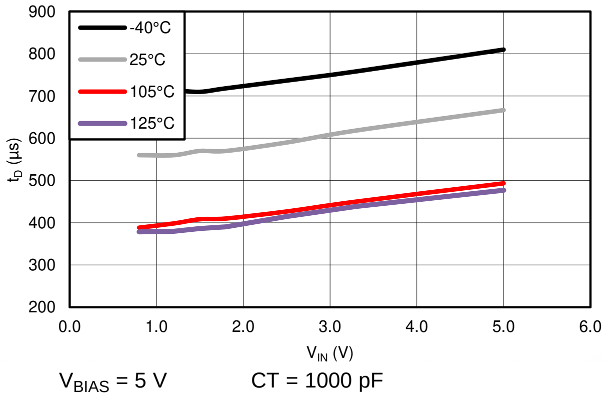


Figure 15. t_D vs V_{IN}

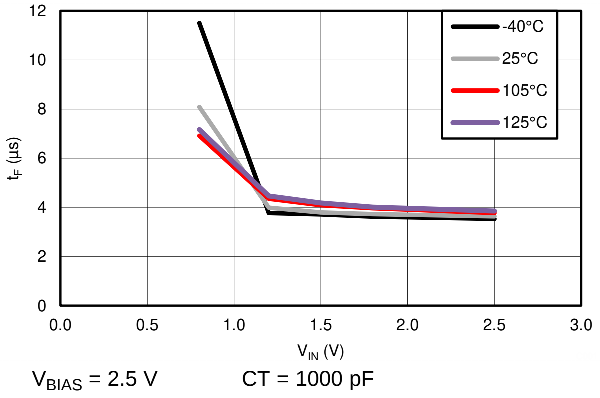


Figure 16. t_F vs V_{IN}

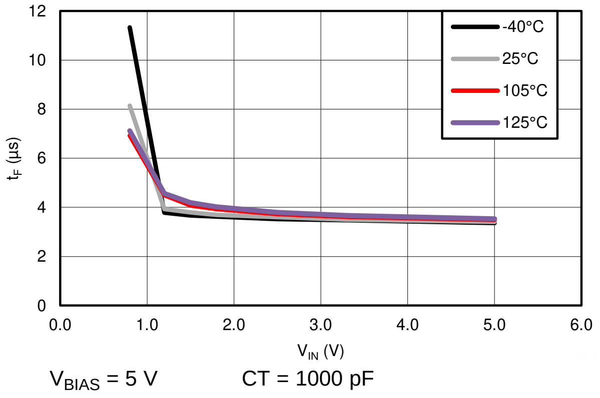
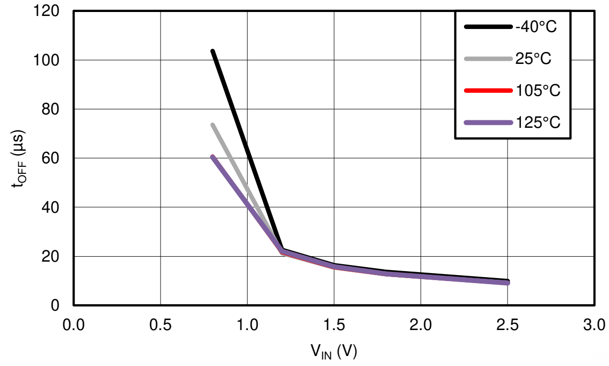


Figure 17. t_F vs V_{IN}

Typical Switching Characteristics (continued)

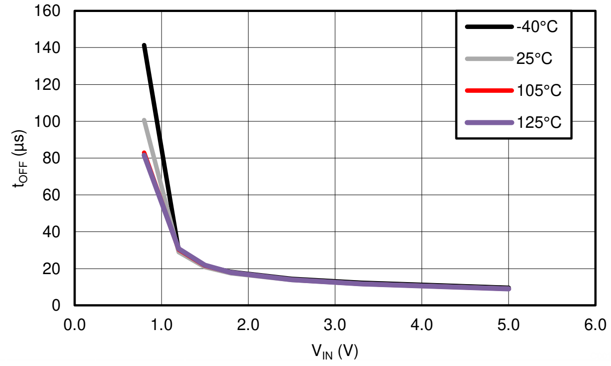
T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



V_{BIAS} = 2.5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

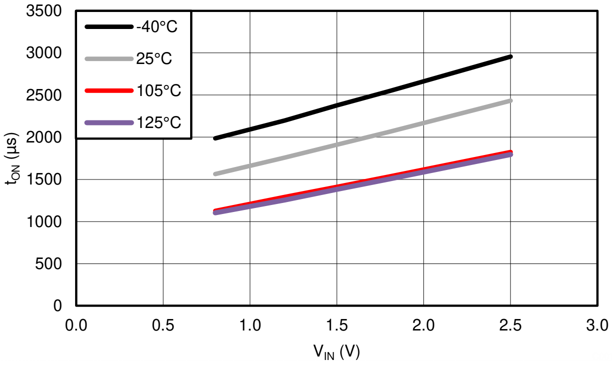
Figure 18. t_{OFF} vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

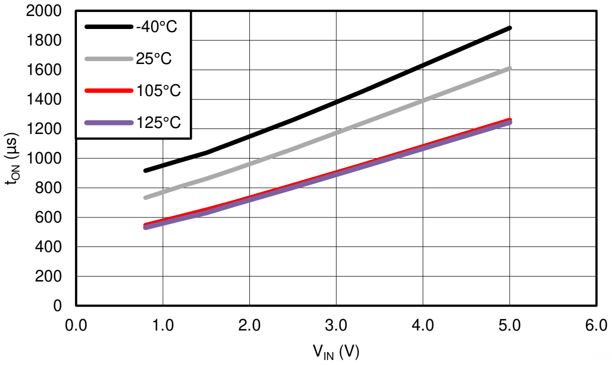
Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 19. t_{OFF} vs V_{IN}



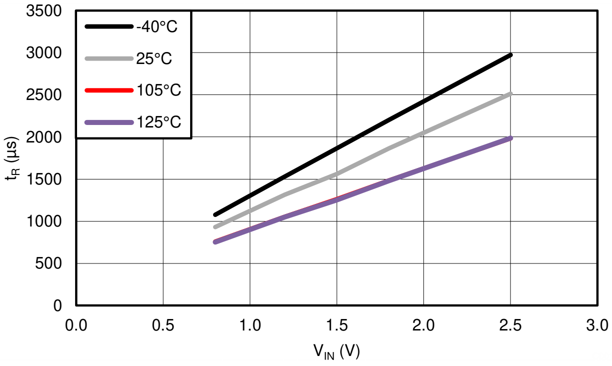
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 20. t_{ON} vs V_{IN}



V_{BIAS} = 5 V CT = 1000 pF

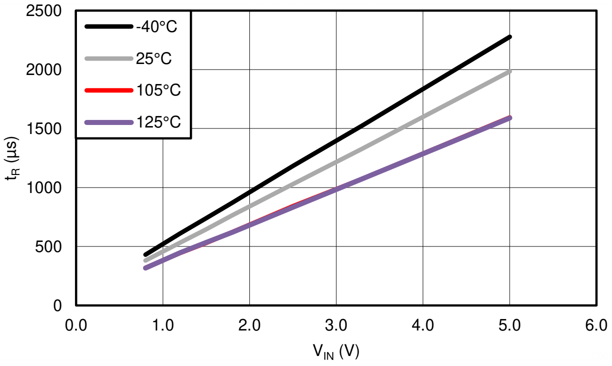
Figure 21. t_{ON} vs V_{IN}



V_{BIAS} = 2.5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 22. t_R vs V_{IN}



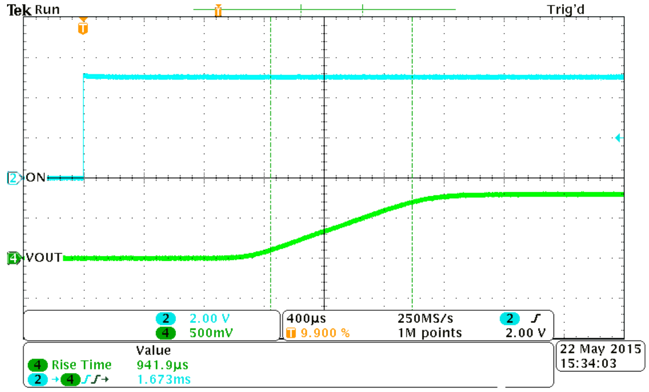
V_{BIAS} = 5 V CT = 1000 pF

Note: The 105°C and 125°C curves have similar values; therefore, only one line is visible.

Figure 23. t_R vs V_{IN}

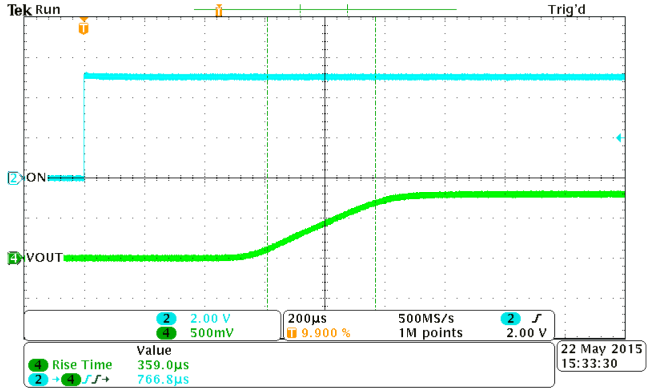
Typical Switching Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



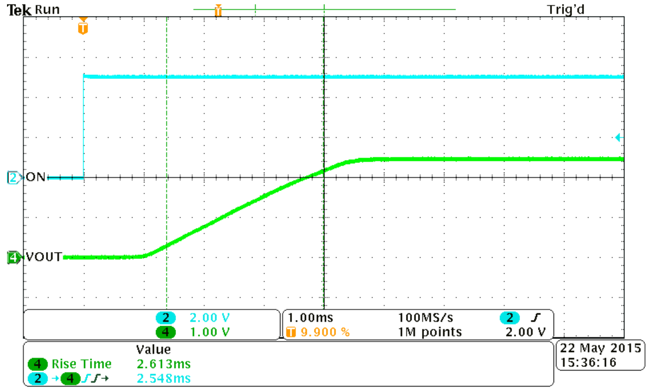
V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

Figure 24. Turnon Response Time



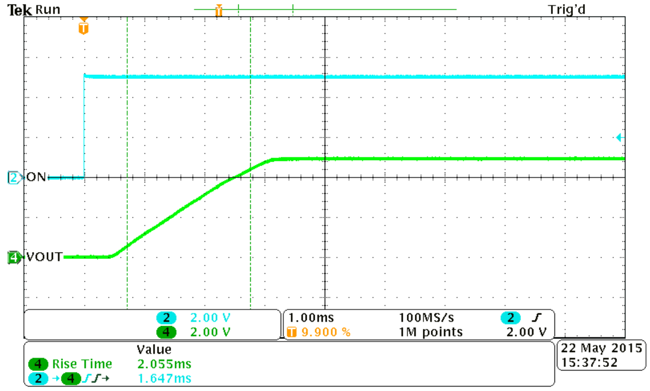
V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

Figure 25. Turnon Response Time



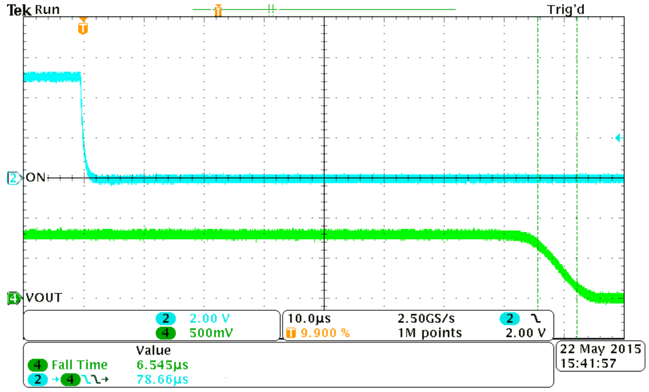
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF,
C_L = 0.1 µF R_L = 10 Ω CT = 1000 pF

Figure 26. Turnon Response Time



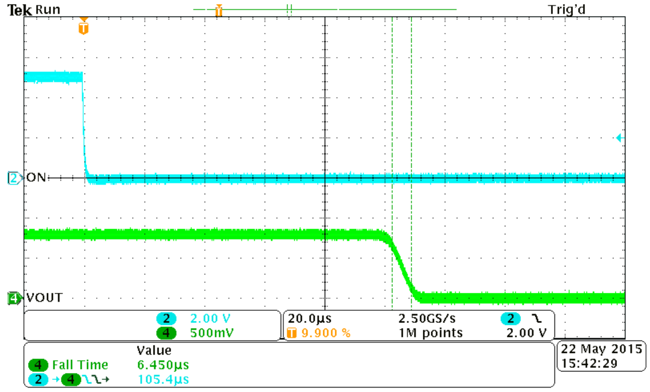
V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 27. Turnon Response Time



V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 28. Turnoff Response Time

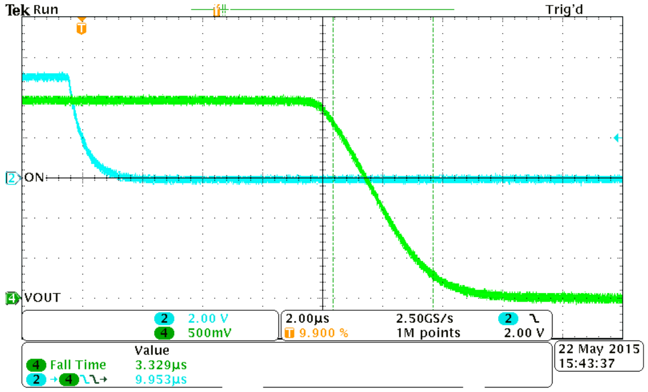


V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 29. Turnoff Response Time

Typical Switching Characteristics (continued)

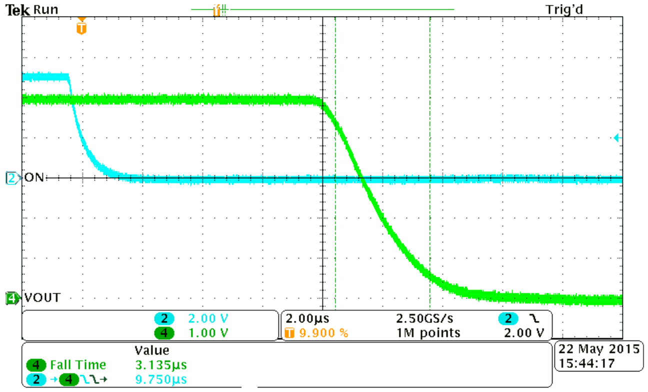
T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω (unless otherwise specified). T_A = 125°C data is only applicable to TPS22965NW-Q1 and TPS22965W-Q1.



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω

Figure 30. Turnoff Response Time

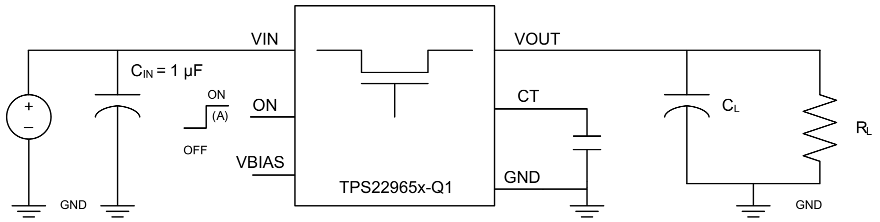


V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF

C_L = 0.1 µF R_L = 10 Ω)

Figure 31. Turnoff Response Time

8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns.

Figure 32. Test Circuit

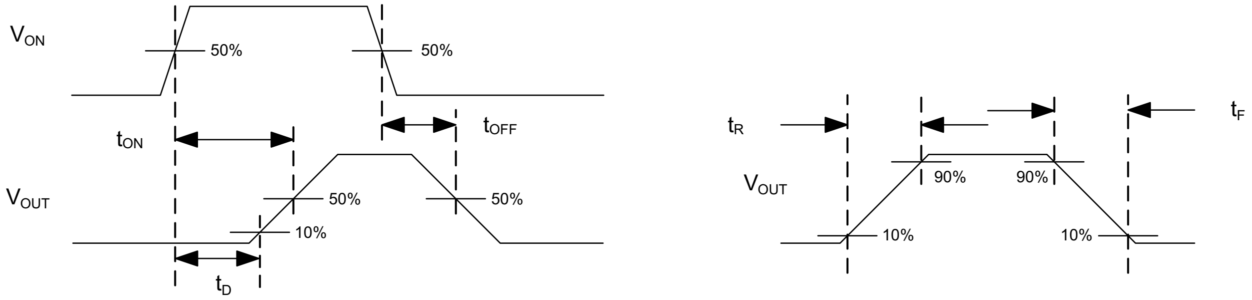


Figure 33. t_{ON} and t_{OFF} Waveforms

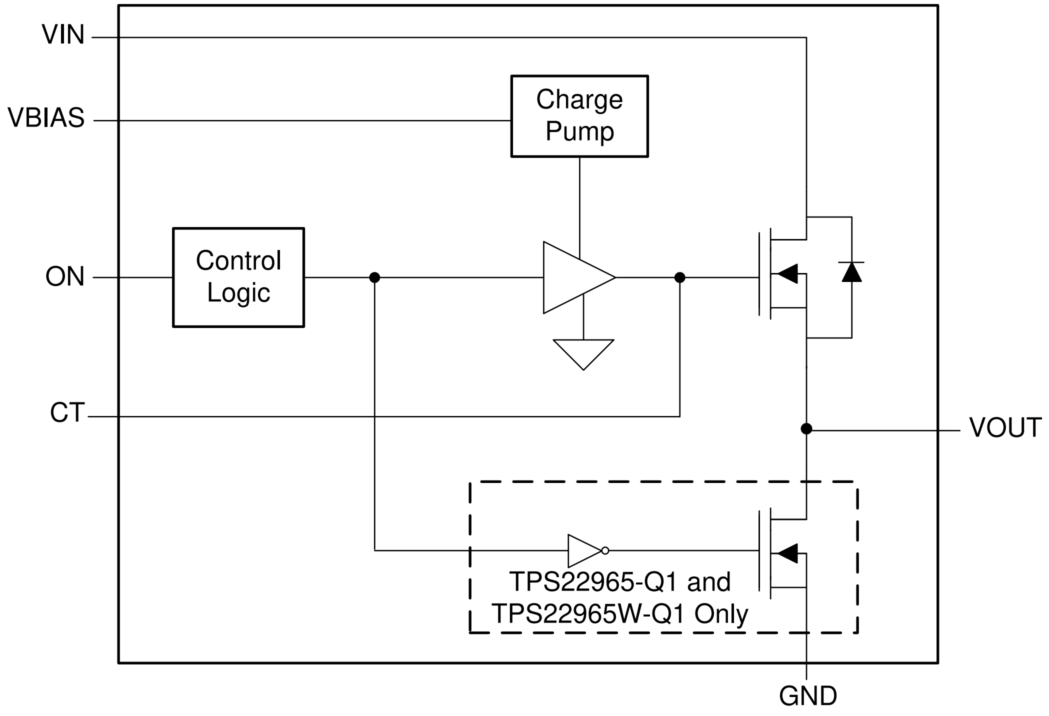
9 Detailed Description

9.1 Overview

The TPS22965x-Q1 is a single channel, 4-A load switch in an 8-pin WSON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V. Therefore, the minimum voltage rating for the CT cap must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0 pF. Use Table 1 to determine rise times for when CT = 0 pF.

$$SR = 0.38 \times CT + 34$$

where

- SR = slew rate (in µs/V)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 34 are µs/V. The units for the constant 0.38 are µs/(V × pF). (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. The rise times listed in Table 1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs CT Capacitor

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V [(1)]						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	180	136	94	84	74	70	60
220	547	378	232	202	173	157	129
470	962	654	386	333	282	252	206
1000	1983	1330	765	647	533	476	382
2200	4013	2693	1537	1310	1077	959	766
4700	8207	5490	3137	2693	2200	1970	1590
10000	17700	11767	6697	5683	4657	4151	3350

(1) Typical Values at 25°C with a 25-V X7R 10% Ceramic Capacitor on CT

9.3.2 Quick Output Discharge (TPS22965-Q1 and TPS22965W-Q1 Only)

The TPS22965-Q1 and TPS22965W-Q1 include a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

9.3.3 Low Power Consumption During Off State

The I_{SD} V_{IN} supply current is 0.01 µA typical at 1.8 V VIN. Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

9.4 Device Functional Modes

Table 2 lists the VOUT pin state as determined by the ON pin.

Table 2. Functional Table

ON	TPS22965N-Q1 AND TPS22965NW-Q1	TPS22965-Q1 AND TPS22965W-Q1
L	Open	GND
H	VIN	VIN

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

10.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the *Electrical Characteristics—V_{BIAS} = 2.5 V* table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 2 to calculate the VIN to VOUT voltage drop.

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination (2)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.1.2 On and Off Control

The ON pin controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.3 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

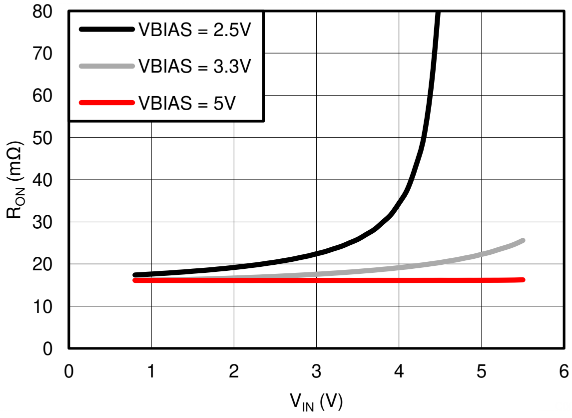
10.1.4 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a $C_{I\ N}$ greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.1.5 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 2.5 V* table. See Figure 34 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

Application Information (continued)



I_{OUT} = –200mA T_A = 25°C

Figure 34. R_{ON} vs. V_{IN} (V_{IN} > V_{BIAS})

10.2 Typical Application

This application demonstrates how the TPS22965x-Q1 can be used to power downstream modules.

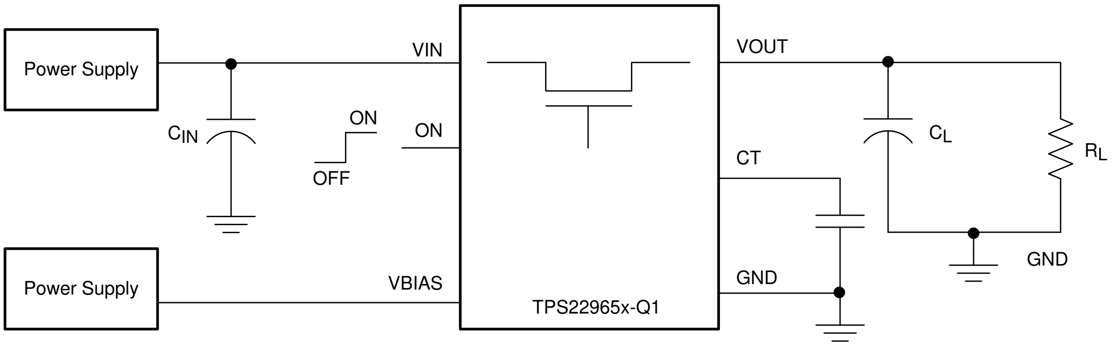


Figure 35. Schematic for Powering a Downstream Module

10.2.1 Design Requirements

Use the values listed in Table 3 as the design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 3.

$$\text{Inrush Current} = C \times dV/dt \tag{3}$$

where

- C = output capacitance
- dV = output voltage
- dt = rise time

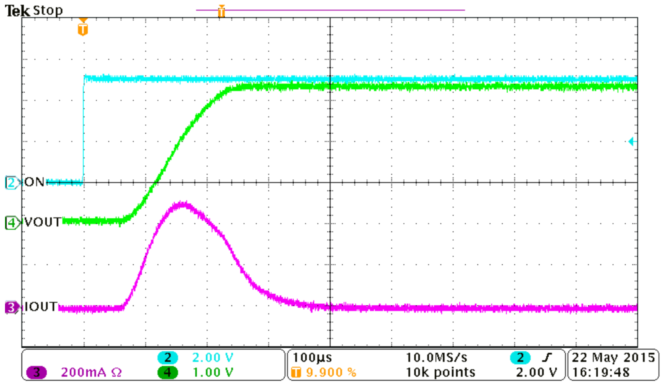
The TPS22965x-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See Equation 4 and Equation 5.

$$400\ \text{mA} = 22\ \mu\text{F} \times 3.3\ \text{V} / dt \tag{4}$$

$$dt = 181.5\ \mu\text{s} \tag{5}$$

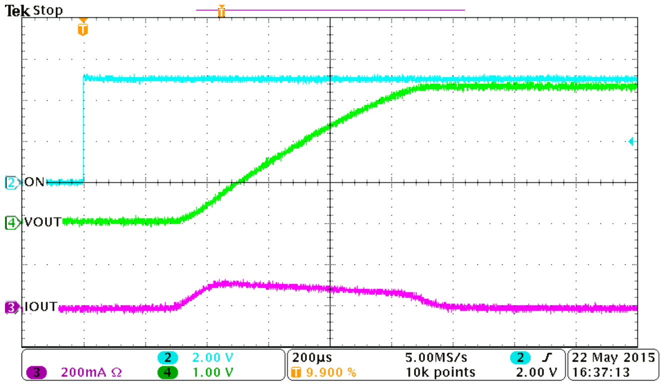
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 36. Inrush Current with CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 37. Inrush Current with CT = 220 pF

11 Power Supply Recommendations

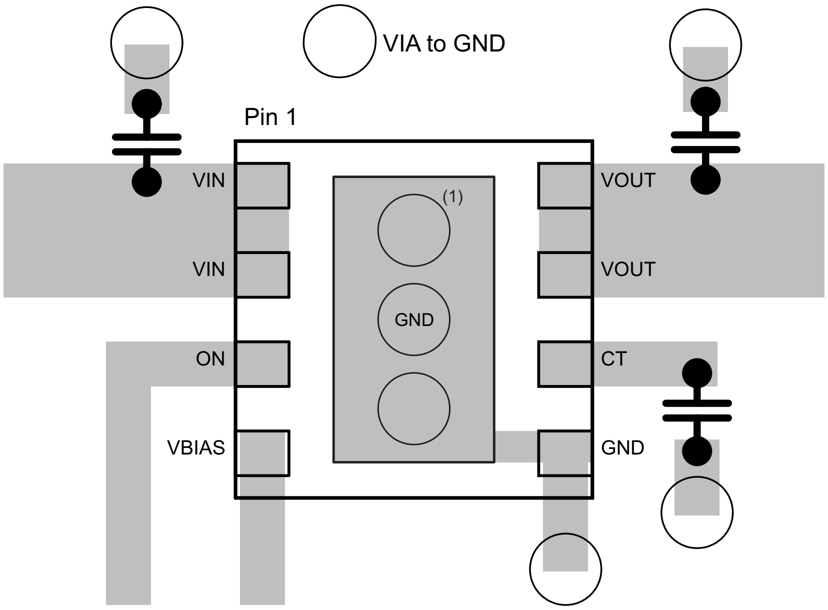
The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN range of 0.8 V to VBIAS.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

12.2 Layout Example



(1) Thermal relief vias. Thermal relief vias connected to the exposed thermal pad

Figure 38. Layout Recommendation

12.3 Thermal Consideration

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 6 as a guideline.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{6}$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22965x-Q1)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout (6)

Refer to Figure 38, notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- *《负载开关：什么是负载开关？为什么需要负载开关？如何选择合适的负载开关？》*
- *《负载开关热效应注意事项》*
- *《管理浪涌电流》*
- *《TPS22965WDSGQ1EVM 5.7V、4A、16mΩ 导通电阻负载开关》*

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22965NQWDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	11B	Samples
TPS22965NQWDSGTQ1	ACTIVE	WSON	DSG	8	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	11B	Samples
TPS22965NTDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZDXI	Samples
TPS22965QWDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	11A	Samples
TPS22965QWDSGTQ1	ACTIVE	WSON	DSG	8	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	11A	Samples
TPS22965TDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE	Samples
TPS22965TDSGTQ1	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZYE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22965-Q1 :

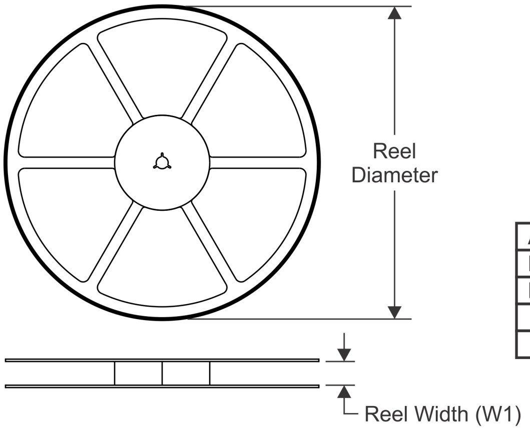
- Catalog : TPS22965

NOTE: Qualified Version Definitions:

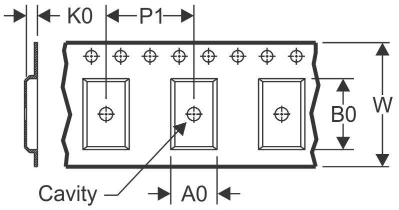
    - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

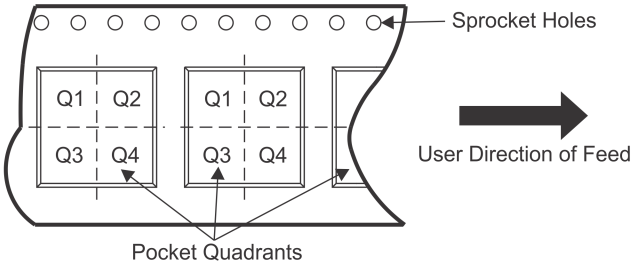


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

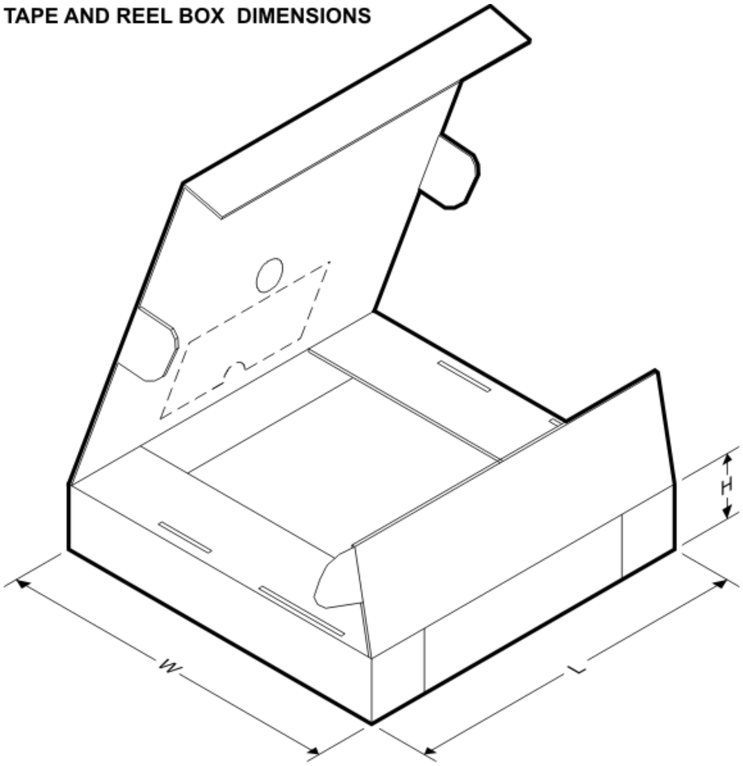
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NQWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965NTDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965QWDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965QWDSGTQ1	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS22965TDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965TDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965NQWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TPS22965NQWDSGTQ1	WSON	DSG	8	250	213.0	191.0	35.0
TPS22965NTDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965QWDSGRQ1	WSON	DSG	8	3000	213.0	191.0	35.0
TPS22965QWDSGTQ1	WSON	DSG	8	250	213.0	191.0	35.0
TPS22965TDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965TDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

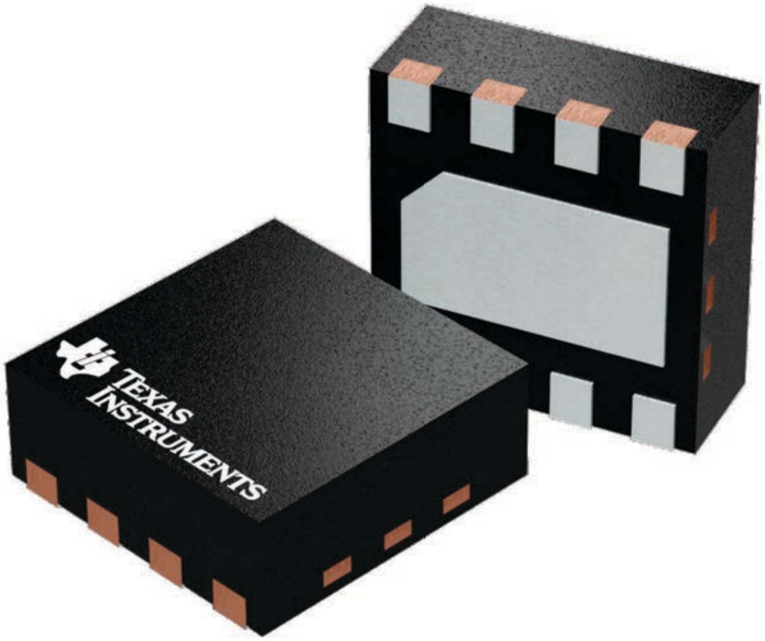
DSG 8

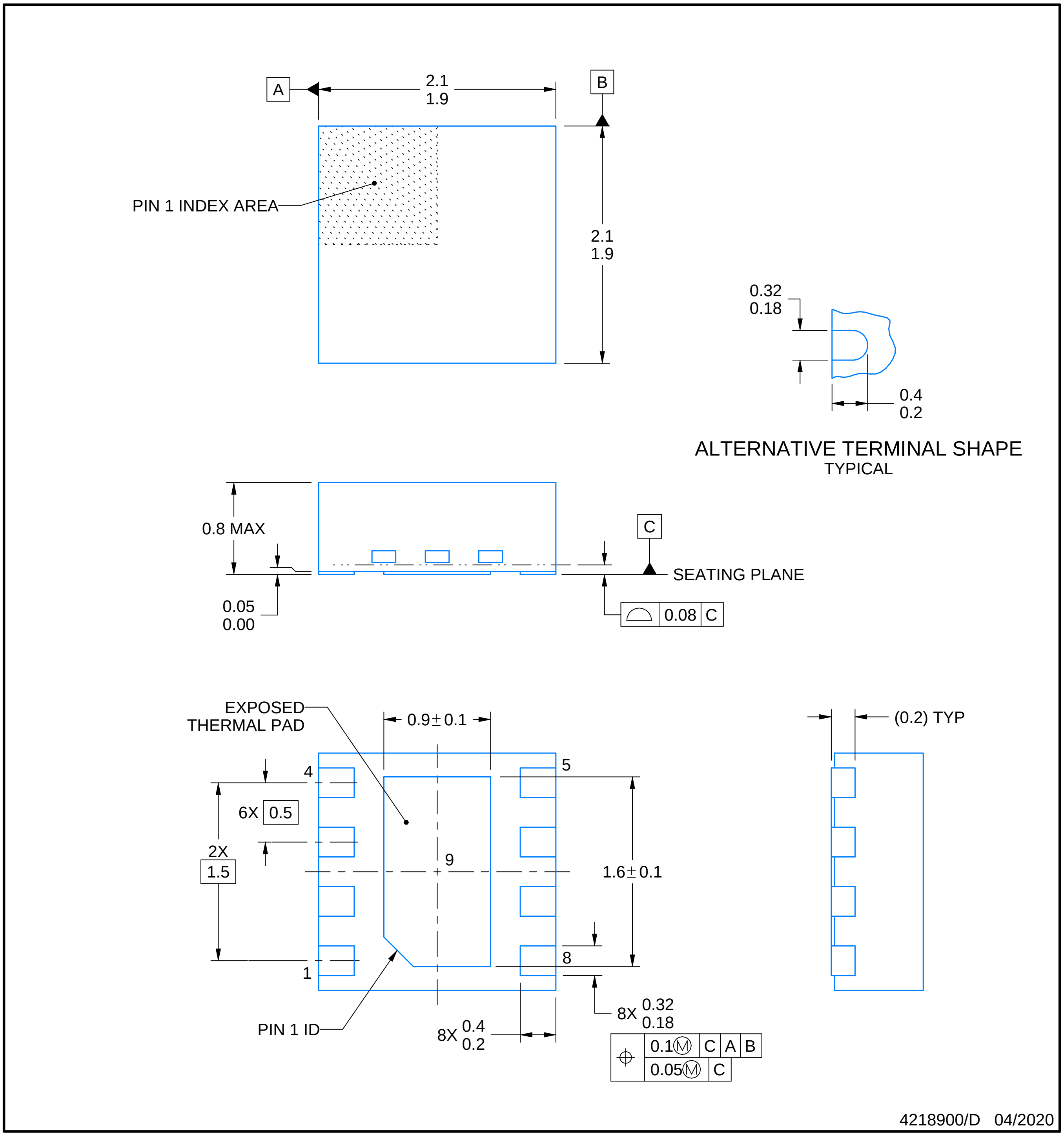
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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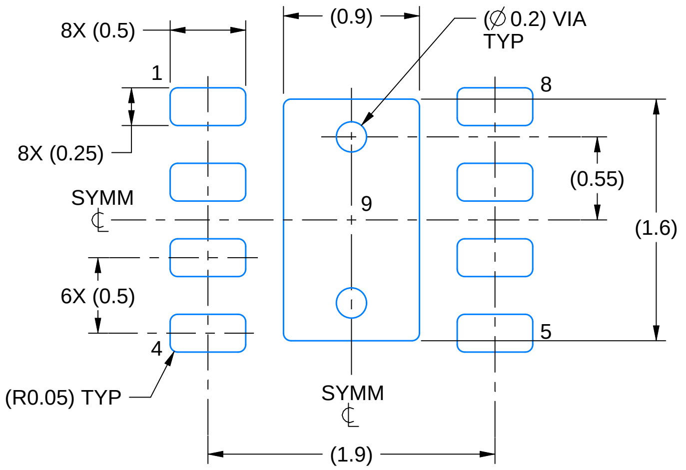
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

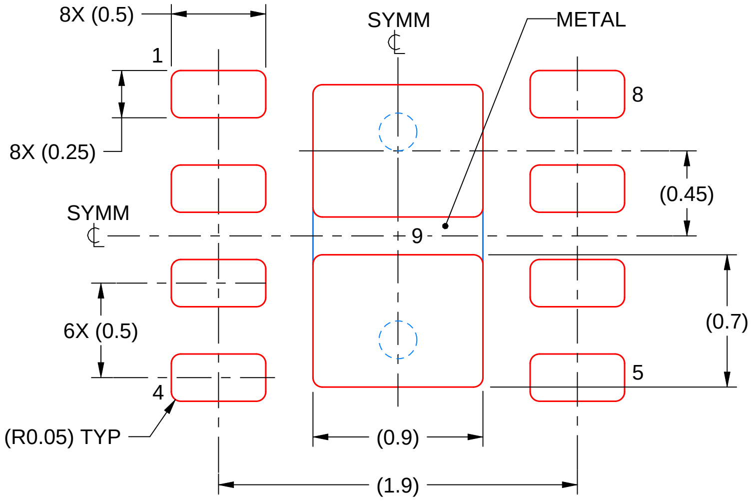
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

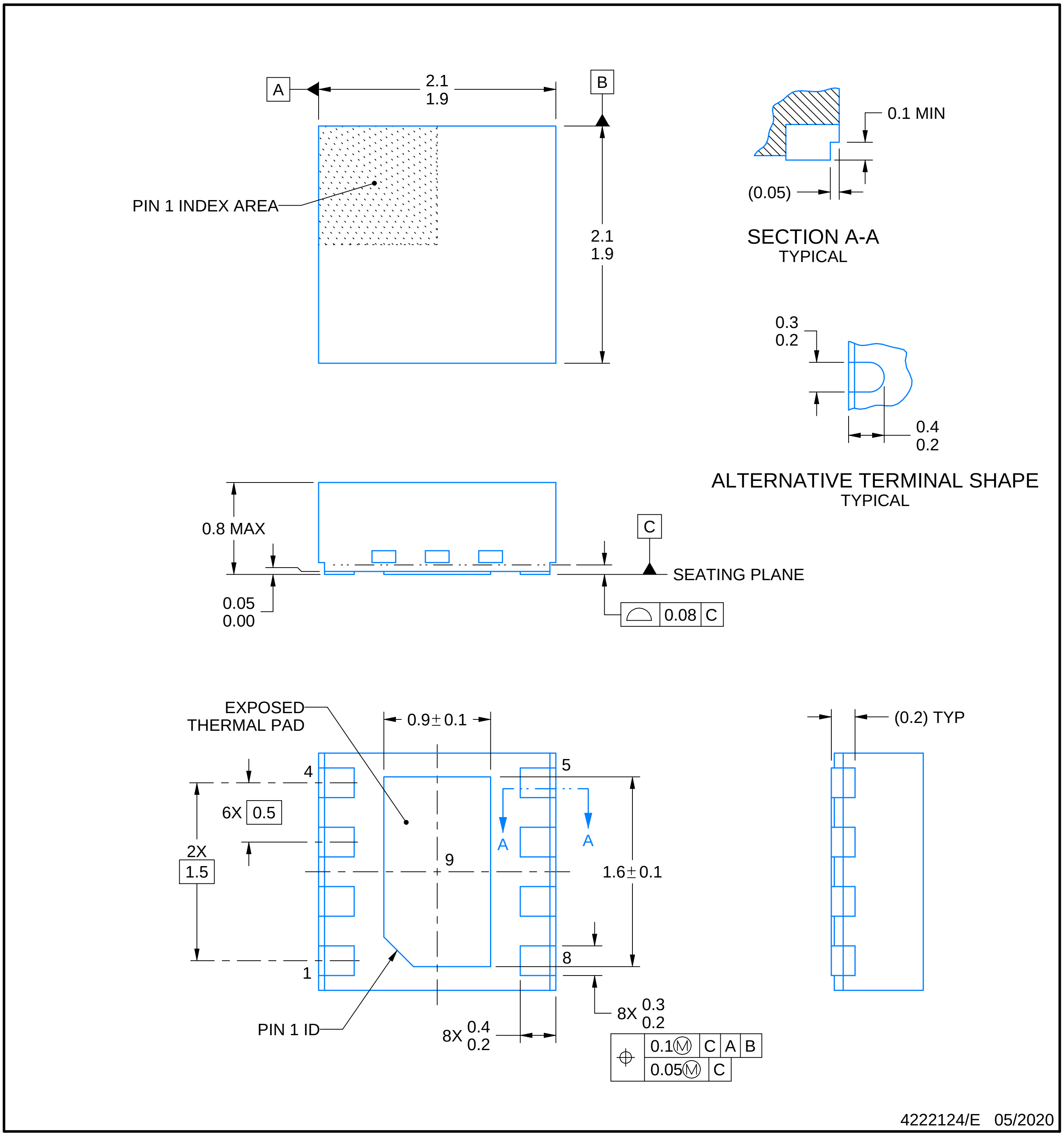


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

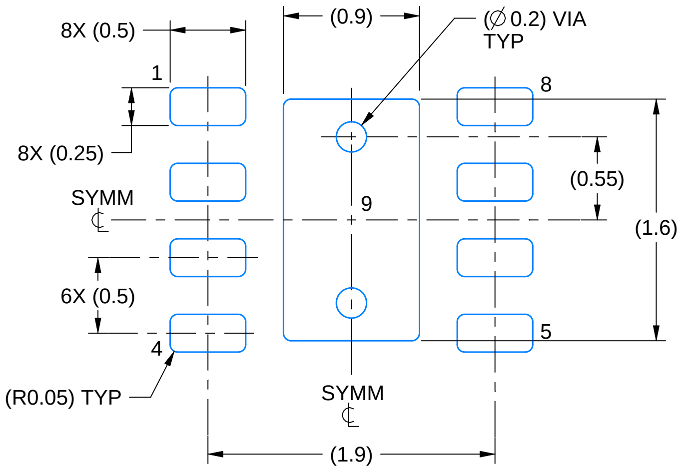
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

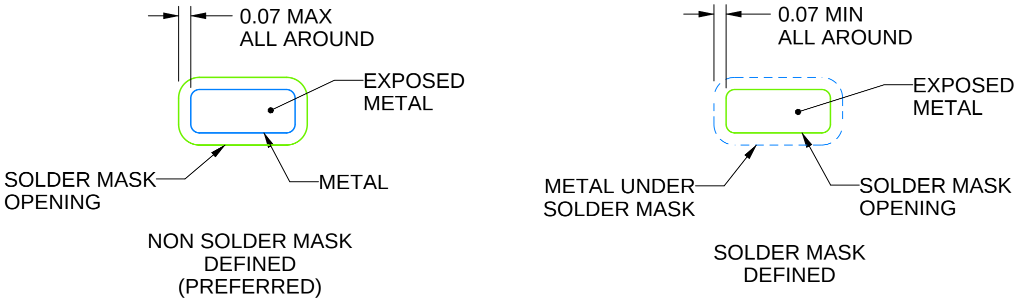


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



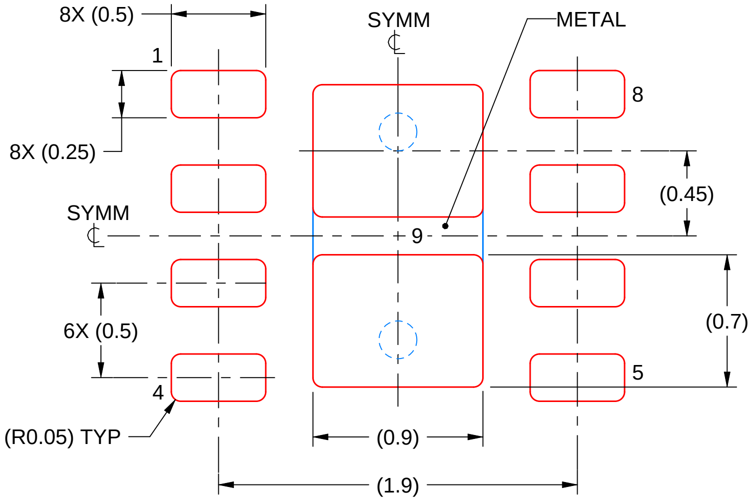
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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